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10/050,002	01/15/2002	Mark Pavier	IR-1837	5495

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EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/050,002	Applicant(s) PAVIER, MARK	
	Examiner Chris C. Chu	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12 - 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12 - 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on December 23, 2003 has been entered. An action on the RCE follows.

Response to Amendment

2. Applicant's amendment filed on December 19, 2003 has been received and entered in the case.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 12, 15 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirasawa et al. '839 in view of Rostoker '771.

Regarding claim 12, Hirasawa et al. discloses in e.g., Fig. 2A, Fig. 2B and column 3, line 33 – column 4, line 52 a semiconductor device comprising:

- a lead frame (201), said lead frame including a conductive die pad (201a) consisting of a conductive material (because the element 201a is formed by only one conductive material) and having a first major surface and a second major surface opposite said first major surface, and a first plurality of leads (201b, at the right-side) disposed at a first edge of said conductive die pad and a second plurality of leads (201b, at the left-side) disposed at a second edge of said conductive die pad, said second edge of said conductive die pad being opposite to said first edge of said conductive die pad;
- a first semiconductor die (206) having a first major electrode (pads on the element 206 which is connected to the element 209a) of a first functionality disposed on a first major surface thereof, and said first major electrode of said first semiconductor die being mounted and electrically connected (through the element 210; column 4, lines 14 - 34) to said first major surface of said conductive die pad (201a);
- a second semiconductor die (206a) having a first major electrode (pads on the element 206a which is connected to the element 209a) of a first functionality disposed on a first major surface thereof and said first major electrode of said second semiconductor die being mounted and electrically connected (through the element 210a; column 4, lines 20 - 34) to said second major surface of said conductive die pad (201a); and

- a molded housing (609 in Fig. 6; column 4, lines 35 - 40) encapsulating said conductive die pad, said first semiconductor die, said second semiconductor die, and portions of said first plurality of leads and said second plurality of lead;
- wherein said conductive die pad (201a) is electrically connected (column 4, lines 14 - 34) to one of said second plurality of leads or one of said first plurality of leads, such that said first major electrode of said first semiconductor die is electrically connected by said conductive material of said conductive die pad to said first major electrode of said second semiconductor die and to said at least one of said second plurality of leads or one of said first plurality of leads.

Hirasawa et al. does not disclose first and second semiconductor dice having a second major electrode of a second functionality disposed on a second major surface, opposite of the first major surface thereof; and wherein said second major electrode of said first and second semiconductor dice are electrically connected to one of said first plurality of leads or one of said second plurality of leads. However, Rostoker teaches in e.g., Fig. 1a and Fig. 1b a semiconductor die (102) having a second major electrode (108) of a second functionality disposed on a second major surface (102b), opposite of the first major surface (102a) thereof and wherein the second major electrode (108) of the semiconductor die is electrically connected to one of first plurality of leads (112a, at the right-side) or one of second plurality of leads (112a, at the left-side). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Hirasawa et al. by adding the second major electrodes of the semiconductor die of Rostoker to the first and second semiconductor dice of Hirasawa et al. and the electrical connections between the second major electrodes and the leads as taught by Rostoker. The

ordinary artisan would have been motivated to modify Hirasawa et al. in the manner described above for at least the purpose of (1) providing high I/O semiconductor dies which has greater than "n" bond sites for connecting to a die (column 3, lines 13 - 43); (2) increasing design freedom in choosing a particular type of chips employed in particular layout; and (3) selecting optimal wiring/interconnect layout.

Regarding claim 15, Hirasawa et al. discloses in e.g., Fig. 2A, Fig. 2B and column 3, line 33 – column 4, line 52 the first plurality of leads including four spaced leads, and said second plurality of leads including four spaced leads.

Regarding claim 19, Hirasawa et al. discloses in e.g., Fig. 2A, Fig. 2B and column 3, line 33 – column 4, line 52 said first plurality of leads being spaced from said conductive die pad and said second plurality of leads being spaced from said conductive die pad.

5. Claims 13, 14 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirasawa et al. and Rostoker as applied to claim 12 above, and further in view of Munoz et al. '910.

Regarding claim 13, Hirasawa et al. and Rostoker disclose the claimed invention except for one of said first semiconductor die and said second semiconductor die being a MOSFET. Munoz et al. discloses in column 2, lines 31 and 32 a semiconductor die being MOSFET. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Hirasawa et al. by using the MOSFET to one of the first and second semiconductor dice as taught by Munoz et al. The ordinary artisan would have been motivated to

further modify Hirasawa et al. in the manner described above for at least the purpose of providing the simultaneous formation of the necessary junctions (column 1, lines 8 ~ 16).

Regarding claim 14, Hirasawa et al. and Rostoker disclose the claimed invention except for the first and second semiconductor dice including a control electrode on said second major surface thereof. Munoz et al. discloses in Fig. 2 and column 2, lines 31 ~ 41 a control electrode (12) on the second major surface of a semiconductor die (10). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Hirasawa et al. by using the control electrode on the second major surface of the first and second semiconductor dice as taught by Munoz et al. The ordinary artisan would have been motivated to further modify Hirasawa et al. in the manner described above for at least the purpose of increasing an area of a package (column 2, lines 50 ~ 51).

Regarding claim 16, Hirasawa et al. and Rostoker disclose the claimed invention except for the first major electrode being a drain electrode of a MOSFET die and the second major electrode being a source electrode of a MOSFET die. Munoz et al. discloses in Fig. 2 and column 2, lines 31 ~ 41 a first major electrode (13) being a drain electrode of a MOSFET die and the second major electrode being a source electrode (11) of a MOSFET die. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Hirasawa et al. by using the drain electrode and the source electrode of a MOSFET die as taught by Munoz et al. The ordinary artisan would have been motivated to further modify Hirasawa et al. in the manner described above for at least the purpose of providing the simultaneous formation of the necessary junctions (column 1, lines 8 ~ 16).

6. Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirasawa et al., Rostoker and Munoz et al. as applied to claim 14 above, and further in view of Adishian '636.

Regarding claim 17, Hirasawa et al. and Rostoker do not disclose each of the first and second semiconductor dice being a MOSFET. However, Munoz et al. discloses in Fig. 2 and column 2, lines 31 ~ 41 a semiconductor die being a MOSFET, said control electrode being a gate electrode (12), said first major electrode being a drain electrode (13), and said second major electrode being a source electrode (11). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Hirasawa et al. by selecting each of the first and second semiconductor dice to be the MOSFET, and the control electrode being the gate electrode, the first major electrode being the drain electrode and the second major electrode being the source electrode as taught by Munoz et al. The ordinary artisan would have been motivated to further modify Hirasawa et al. in the manner described above for at least the purpose of providing the simultaneous formation of the necessary junctions (column 1, lines 8 ~ 16).

Furthermore, Hirasawa et al., Rostoker and Munoz et al. does not disclose said gate electrodes of said MOSFETs being electrically connected to one of said plurality of second leads, said source electrodes of said MOSFETs being electrically connected to another one of said second plurality of leads, and said conductive die pad being electrically connected to the remaining leads of said second plurality of leads, and the source electrodes of said MOSFETs being also connected to said first plurality of leads. Adishian discloses in Fig. 1 ~ Fig. 5 and column 2, line 37 the gate electrodes (G1, G2, etc.) of the MOSFETs being electrically

connected to one of the plurality of second leads (24), the source electrodes (S1, S2, R1, R2, etc.) of the MOSFETs being electrically connected to another one of the second plurality of leads (22), and the conductive die pad (12) being electrically connected to the remaining leads of the second plurality of leads (GA, GB, and GC), and the source electrodes of the MOSFETs being also connected to the first plurality of leads. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to further modify Golwalkar et al. by using the connections between the electrodes and the leads as taught by Adishian. The ordinary artisan would have been motivated to further modify Golwalkar et al. in the manner described above for at least the purpose of providing a structurally, both thermally and electrically optimized and improved very-high-power transistor (column 1, lines 56 ~ 61).

Regarding claim 18, Hirasawa et al. and Rostoker disclose at least one electrical connection being made by wire bonding.

Response to Arguments

7. Applicant's arguments with respect to claim 12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 517-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

c.c.
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BRADLEY BAUMEISTER
PRIMARY EXAMINER